REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-6 remain in the application. Claim 1 has been amended. Claims 7-8 have been cancelled.

In item 2 on pages 2-3 of the above-mentioned Office action, claims 1-8 have been rejected as being anticipated by Lanzerstorfer et al. (US Pat. No. 6,605,841 B2) under 35 U.S.C. § 102(b).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in paragraphs [0035] and [0051] of allowed U.S. Application No. 10/392,024, the content of which has been incorporated into the instant application, and original claims 7 and 8.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a field electrode extending in said trench substantially from said trench base to an upper edge of said first

dielectric layer, said field electrode being connected to be at a fixed potential or at a source potential;

a gate electrode disposed substantially between said body height and the semiconductor body surface, said gate electrode being electrically insulated from the semiconductor body by said gate oxide and having a lower edge with a profile at least partly different from horizontal.

The invention of the instant application pertains to trench transistor cells with a vertical channel and gate electrodes provided in trenches. A field electrode, which is insulated from the gate electrode and which shields the gate electrode from the drain electrode, is disposed below the respective gate electrode in the trench.

The invention of the instant application is based on a particular embodiment of a dielectric intermediate layer which is disposed between the field electrode and the gate electrode, which has the effect that the adjustment of the lower edge of the gate electrode to a pn-junction in the surrounding semiconductor substrate is simplified in a production engineering manner. The permissible distance between the lower edge of the gate electrode and the pn-junction is increased.

Lanzerstorfer et al. pertain to a method for simultaneous production of a gate electrode for a trench transistor cell as

well as for a gate electrode of a planar transistor cell on the same semiconductor substrate.

The (planar) gate electrode of the planar transistor cell is to be provided in a much thinner manner than is necessary for the complete filling of the gate trenches. Lanzerstorfer et al. thus provide initial application of a first section of a gate conductor layer in a layer thickness that corresponds the desired layer thickness of the planar gate electrode. The gate trenches are only partly filled by the first section of the gate conductor layer. In a second step, an intermediate layer is applied on the gate conductor layer. A second section of the gate conductor layer is deposited on the intermediate layer so that the trenches are filled completely.

In the following step, the second section of the gate conductor layer is etched in the region of the vertical transistor structures reaching back into the trenches. In the region of the planar transistor structures, the intermediate layer works as an etching stop layer.

After removal of the etching stop layer, the first section of the gate conductor layer forms the planar gate electrodes in the desired thin layer thickness; the gate trenches are filled completely with the first section 40 and second sections 60 of

the gate conductor layer, which are separated from each other by the retentive sections of the intermediate layer.

The two sections 60 and 40 of the gate electrode of Lanzerstorfer et al. are connected with each other and are thus controlled together by a gate potential.

The transistor configuration according to the invention of the instant application differs from the configuration known from the prior art reference in the following aspects:

a) In the invention of the instant application, the gate electrode is insulated from the semiconductor substrate exclusively by the gate oxide. In the transistor configuration of Lanzerstorfer et al., the second gate electrode section 60 is insulated from the semiconductor layer by the intermediate layer 50, the first gate electrode section 40, and the gate oxide 22 due to production conditions.

> *"[said gate electrode] being electrically insulated from the semiconductor body [substrate] by the gate oxide [first gate dielectric layer]"*

The feature is disclosed in the figures of the instant application as well as in paragraphs [0035] and [0051] of allowed U.S. Application No. 10/392,024, the content of which

has been incorporated into the instant application (see page 15 of the specification of the instant application).

b) The different control of the "field electrode" and the "gate electrode."

According to column 6, line 50 and following portions of Lanzerstorfer et al., the two partial sections of the gate electrode are placed at the same potential and work as a common gate electrode of the vertical transistor element. It becomes clear from column 6, line 57 and following portions that both partial sections together form the gate electrode and that they are controlled together. The same also holds true according to column 6, line 63 and following portions.

According to the invention of the instant application, however, the field electrode is connected to the source potential or to a fixed potential.

> *"the field electrode being connected to be at a fixed potential or at a source potential"*

Clearly, Lanzerstorfer et al. do not show "a field electrode extending in said trench substantially from said trench base to an upper edge of said first dielectric layer, said field

electrode being connected to be at a fixed potential or at a source potential; a gate electrode disposed substantially between said body height and the semiconductor body surface, said gate electrode being electrically insulated from the semiconductor body by said gate oxide and having a lower edge with a profile at least partly different from horizontal," as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over Lanzerstorfer et al. and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-6 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150

Yonghong Chen
For Applicants

YC

December 30, 2004

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101